Multifunctional Information Distribution System (MIDS)
White Wires On Printed Circuit Boards

PROBLEM / OBJECTIVE

Multifunctional Information Distribution System (IDS) is a terminal that provides communications, navigation, and identification capabilities to host platforms in support of key theater functions such as surveillance, identification, air control, weapons engagement, coordination, and direction for all Services, North Atlantic Treaty Organization (NATO) forces, and selected other allies. The system is to provide a high throughput line-of-sight jam-resistant communications to host platforms.

The printed circuit boards employed in MIDS require a robust mature design with no room for error. White wires on printed circuit boards are added features after the design is finished and represent potential points of failure. For optimum performance all white wires should be eliminated from the assembly to reduce potential failure mechanisms.

ACCOMPLISHMENTS / PAYOFF

Contractor Control:

Championed by BMP the MIDS Program Office pursued a zero white wire count on all printed circuit boards manufactured for MIDS. The contractors reviewed board designs that included white wires and executed redesign in areas that proved to be advantageous to system cost and performance. With "buy-in" from participating contractors, white wires were reduced to an acceptable risk.

Implementation and Technology Transfer:

MIL-C-28809B had been the guideline document for white wire applications. Best Commercial Practices have discontinued and superceded this document. Relying on Best Commercial Practices, participating contractors followed standard operating processes that include documenting design requirements, test analyze and fix, production planning, regression testing new design and, finally, performing an Acceptance Test Procedure (ATP) on the board. Once this is successfully completed, board laminas are re-spun to reduce production costs and increase assembly reliability.

SRU/CCA	White Wire Qty	
	FAQT/LOT 1	**Lot 2**
PAI Total	Up to 25	Up to 2
Exciter/IPF Total	Up to 25	Up to 1
RTI/Disc Total	Up to 3	Up to 3
RPS	Up to 33 or 20**	Up to 1
Signal Message Processor Total	Up to 3	Up to 3
TACAN Mod. Assy Total		
DP/Amux Total	Up to 8	Up to 8
TP/Gmux Total	Up to 11	Up to 10

Expected Benefits:

The elimination of white wires on printed circuit boards will improve assembly robustness and ultimately increase Fleet availability of MIDS terminals. In addition, spares provisioning and depot rework and repair costs will be reduced.

TIME LINE / MILESTONE

Start Date: October 2001
End Date: September 2002

FUNDING

Navy ManTech: $0.800M
MIDS IPO: $0.250M

PARTICIPATING CONTRACTORS

BAE Systems
Rockwell Collins
ViaSat, Inc
Harris Corp.
Xetron